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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,508	12/21/2004	Patrick Ward	26533U	8383
20529	7590	12/28/2005		EXAMINER
				ZHU, JOHN X
			ART UNIT	PAPER NUMBER
				2858

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/518,508	WARD, PATRICK
Examiner	Art Unit	
John Zhu	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

1) Responsive to communication(s) filed on 01 December 2005.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

4) Claim(s) 1-9 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-9 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 12/21/2004 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

1. Response to communication filed 12/01/2005.

### *Drawings*

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
4. Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 2 each contain the amended limitation of *onset* of the first and second signals. No support for this limitation is found in the specification or drawings.

Claims 3-9 and claims depend therefrom (claims 1 and 2) fails to comply with the written description requirement.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 3, 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Ahuja (5,388,022).

With respect to claims 1,2 and 3, AAPA discloses a residual current detection circuit comprising means for detecting an imbalance current and providing an output (Output of FWR, fig. 2) whose amplitude corresponds to the magnitude of the residual current. Furthermore, AAPA discloses capacitor (Fig. 2, element C2), which acquires a charge corresponding to the amplitude of the output and provides that signal via a parallel resistor (Fig. 2, element R5).

AAPA does not disclose simultaneously applying the output the detected current to two channels with the onset of the signal of one of the channels is time delayed with respect to the onset of the first signal and providing a final output signal through an AND

gate only when the first signal exceeds a first level at the input of the AND gate and a second signal corresponding to the amplitude of the voltage on the capacitor exceeding a second level at the other input of the AND gate. AAPA also does not disclose the circuit stage producing an output only if the duration of the first signal (duration read as one or more fluctuations) is greater than the delay in the onset of the second signal.

Ahuja discloses an auto reset circuit breaker that utilizes simultaneous providing a first and second channel (Fig. 1, node 25) wherein the onset of the signal of the second channel is time delayed with respect to the onset of the first signal, and passed to an AND gate (Fig. 1, element 30) that outputs a trip signal only when both signals are coincident, which inherently means only if the duration of the first signal is greater than the delay in the onset of the second signal.

It is known that AND gates are used in digital logic and inherently possess threshold values at inputs that corresponds to logic high or low values. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the two channels coupled to an AND gate as taught by Ahuja into the system of AAPA for the purpose of automatically controlling the reset switch when the trip voltage values and current drop below a specified predetermined value (Ahuja, column 2, lines 12-15).

With respect to claims 4 and 9, AAPA disclose the output of the full wave rectifier as a voltage value. Furthermore, a circuit analysis of an AND gate confirms that it inherently comprises comparators that compares the values of the inputs, in this case,

the first and second channels, with reference voltages to determine the logic level. As disclosed in the above rejection, the first channel is the output from the full wave rectifier, and the second channel is a time delayed signal of the output of the full wave rectifier. The AND gate also clamps (by outputting logic zeros) the output of the first zero until the occurrence (logic one) of the second signal.

***Allowable Subject Matter***

7. Claims 5, 6, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5, 6, 7 and 8 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Claim 5 is allowable over the art of record because the prior art does not teach or suggest a residual current detector or ground fault detector that comprises charging a second capacitor upon the occurrence of a second comparator output signal followed by a third comparator for comparing the voltage level of the second capacitor with a reference voltage.

Claims 6-8 are allowable as they depend from an allowable claim.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Response to Arguments***

10. Applicant's arguments filed 12/01/2005 have been fully considered but they are not persuasive.

With regards to applicant's arguments regarding claims 1 and 2 on the lack of onset disclosed in the reference, the examiner respectfully disagrees. As shown by Fig. 1c and 1d of the Ahuja reference, the onset of the first signal (read by the examiner as starting at logic 0) is time delay and indicated by Fig. 1d. The onset of the second signal

is shifted to the right (time delayed) and eventually follows the pattern of the first signal (by transitioning from 0 to 1 at a later time).

With regards to applicant's arguments regarding claims 1 and 2 on the lack of limitation of *the circuit stage produces an output only if the duration of the first signal is greater than the delay in the onset of the second signal*, the examiner believes this is an inherent property of the structure as presented. In a comparison of Fig. 1 of Ahuja and Fig. 2 of applicant's application, we see the circuit stage as being identical; an AND gate whose input is coupled to a first signal and a second signal derived from a delay of the first signal. As a person of ordinary skills in the art of electronics will know, an AND gate will produce an output if the inputs are a logic 1. In this case, as the second signal is a time delayed version of the first, the only points in which an output occurs is when the first and second signals overlap (logic 1 overlaps), or in other words, when the duration of the first signal (duration read as one or more fluctuations) is greater than the delay in the onset of the second signal.

#### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Zhu whose telephone number is (571) 272-5920. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on (571) 272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John Zhu  
Examiner  
Art Unit 2858

JZ



DIANE I. LEE  
PRIMARY EXAMINER